Application Note

Document No.: AN1160

G32R501 Hardware Design Guide

Version: V1.1

1 Introduction

G32R501 is a high-performance MCU developed by Geehy for real-time control applications. It is equipped with a Cortex-M52 microprocessor based on the Arm v8.1-M architecture, supports dual-core parallel operation, and implements efficient collaborative processing. Its outstanding performance is suitable for such application scenarios as motion control, photovoltaic inverters, digital power supplies, and on-board chargers (OBC).

This application report provides guidance for hardware development using this device, and focuses on system-level hardware design, device selection, schematic diagram design, and layout recommendations. It is a basic guide for hardware developers, and is conductive to simplifying the design process and reducing the likelihood of design errors. The main topics of the discussion include power supply requirements, general-purpose input/output (GPIO) connection, analog inputs and ADC, clock generation and requirements, and cJTAG/JTAG debugging.

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2 Introduction to G32R501

The maximum operating frequency of G32R501 MCU can be up to 250MHz, realizing custom datapath extension (CDE) for Arm Rv8-M. It is equipped with Helium™ technology based on M-profile vector extension (MVE), which further improves the processing performance through innovative Zidian mathematical instruction extension unit. The Zidian mathematical instruction extension unit set can quickly execute the algorithms that include the common trigonometric operations in transformation and torque loop calculation, and reduce the delay of common complex mathematical operation in coding application.

G32R501 supports up to 640KB Flash internally. The Flash is divided into two independent memory banks of 512KB and 128KB, supporting parallel programming and execution. Besides, through the built-in CFGSMS, efficient system partitioning can be implemented for 128KB SRAM storage on the chip. Each logical block has a size of 8KB (a total of 8), which can be configured for different types of usage, e.g. ITCM, DTCM, and SRAM. In addition, G32R501 also supports Flash ECC, RAM parity, and security attribute configuration.

G32R501 chip integrates high-performance analog unit, which can further improve the system control performance. Three independent 12-bit ADC can accurately and efficiently collect and process multiple analog signals, thereby improving system throughput. 7 comparator subsystems can constantly monitor the input voltage level through the tripping function.

G32R501 includes performance-leading control peripherals (with frequency-independent PWM and CAP/HRCAP), which can place excellent control over the system. The built-in 4-channel SDF is suitable for external isolated Σ-Δ modulators.

The communication ports, including SPI, UART, I2C, LIN, and CAN, are built in G32R501, and multiplexing options are provided to flexibly meet the communication requirements of various applications. The G32R501x device also provides the PMBus interface and high-speed QSPI interface that fully comply with the standards. Besides, G32R501 also supports JTAG, cJTAG, and SWD debugging interfaces. The multiple debugging modes are suitable for different system environments and performance requirements.

G32R501 supports the operating temperatures ranging from -40°C to 105°C/125°C, and provides multiple packages for selection such as QFN56, LQFP64, LQFP80, and LQFP100.

3 Schematic Diagram Design Reference

The following sections outline the key steps for designing the initial schematic diagram using the G32R501 device, covering package selection, device function and peripheral integration, and precautions for improving system and device performance.

3.1 Analog I/O

This section mainly introduces the key precautions for analog signals of G32R501. It introduces key information such as ADC pin selection and analog reference.

3.1.1 Analog peripherals

G32R501 contains different quantities of the following analog peripherals:

- 12-bit analog-to-digital converter (ADC)
- Temperature sensor
- Buffer digital-to-analog converter (DAC)
- Comparator (COMP)

3.1.2 Select analog pins

Like GPIO pins, the analog peripheral provides flexible usage of pins. The buffer DAC output, COMP input, digital input, and ADC input are multiplexed. In addition, all ADC have internal connections to VREFLO, allowing for offset self-calibration.

When selecting analog pin connection, the peripheral functions supported by each pin should be considered. The analog inputs with comparators on some pins enable these analog signals to quickly trigger PWM (as fault signals) or detect zero crossing. Multiple analog signals can be sampled simultaneously to improve the efficiency. For example, three synchronous analog signals can be connected to ADC-A, ADC-B, and ADC-C respectively to achieve simultaneous sampling.

The analog pins of G32R501 are multiplexed with digital GPIO, known as AIO (analog input/output), and they are multiplexed analog pins that can only operate in input mode. By default, when GPIO is in a high-impedance state (high-impedance state), they will be used as analog pins. It is important to note that if a digital signal with sharp edges is connected to the AIO pin, it may cause crosstalk to adjacent analog signals, and affect the signal integrity.

3.1.3 Internal and external analog references

The onboard ADC uses VREFHIx and VREFLOx as voltage references. For most applications, the internal voltage reference can provide sufficiently high performance. Therefore, the voltage of the VREFHIx pin is driven by the internal bandgap voltage reference, and the voltage of this

voltage reference can be selected as 1.65V output (0V to 3.3V) or 2.5V output (0V to 2.5V). If the design of the implemented system requires higher accuracy, the external reference voltage can be used instead.

When the internal reference mode is used, no additional voltage source should be placed on the VREFHIx pin, which is because the device itself will drive the voltage to this pin. In external reference mode, an external circuit (e.g. voltage reference chip or high-speed operational amplifier) is required to provide a reference voltage of 2.4V to VDDA for the VREFHIx pin. Regardless of which mode is used, a 2.2μF capacitor needs to be connected to the VREFHIx pin to ensure the stability (multiple VREFHIx links are on the same pin, and the capacitance increases accordingly).

3.1.4 ADC input

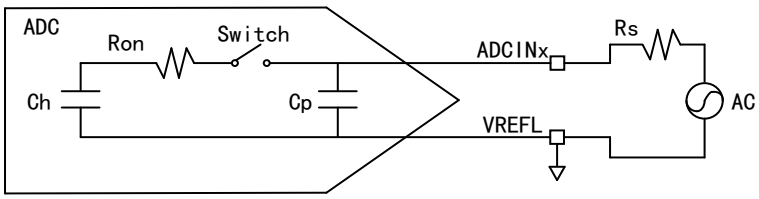
To ensure normal performance of ADC, its input impedance and bandwidth requirements should be designed and evaluated correctly. If these requirements are not met, memory crosstalk and significant stability errors in sample and hold (S+H) circuits may be caused.

Figure 3 shows the ADC input model, which includes the following key parameters:

- Cp: Parasitic input capacitance
- Ron: Sampling switch resistance
- Ch: Sampling capacitance
- Rs: Nominal source impedance

The G32R501 data sheet records the parasitic capacitance of each channel of the ADC, and the parasitic capacitance helps optimize the circuit design to meet performance requirements. In addition, the duration of the acquisition window for each SOC can be adjusted by adjusting ACQPS or reducing the sampling frequency, or by their combination.

Figure 1 ADC Input Model



3.2 Digital I/O

This section introduces the digital signals present in the device, which covers a wide range from GPIO to integrated communication and control peripheral support.

3.2.1 General-Purpose Input/Output

The I/O (GPIO) pins of G32R501 can be configured as typical GPIO or peripheral I/O signals, and the peripheral signals can be multiplexed with general-purpose input/output (GPIO) signals. When resetting, the GPIO pin is configured as input. For specific inputs, users can also choose the number of input qualification periods to filter out unnecessary noise interference.

The GPIO module includes the output X-BAR, which allows routing various internal signals to the GPIO in GPIO multiplexer position and is represented as OUTPUTXBARx. The GPIO module also includes the input X-BAR, which is used to route signals from any GPIO input to different IP blocks, for example ADC, CAP, PWM, and external interrupts.

Each GPIO pin supports a maximum sink current and source current of 6mA, with a maximum output frequency of 60MHz, and a rise/fall time of 8ns.

Figure 2 General-purpose Output Timing

3.2.2 Integrated peripherals and X-BAR

From the above mentioned, each peripheral signal is multiplexed onto many GPIO pins to simplify the design and layout process and achieve maximum flexibility. For detailed peripheral configurations of each GPIO, please refer to the pin attribute table of G32R501.

Input X-BAR is used to route signals from GPIO to many different IP blocks, for example ADC, CAP, PWM, and external interrupts. The output X-BAR has eight outputs, which are routed to GPIO modules.

3.2.3 Control peripherals

G32R501 device contains different quantities of the following control peripherals:

(1) Capture (CAP)

(2) High-resolution capture (HRCAP6-HRCAP7)

(3) Pulse width modulator (PWM)

(4) High-resolution pulse width modulator (HRPWM)

(5) Quadrature encoder pulse (QEP)

(6) Σ-Δ filter module (SDF)

For some low-level analog, high-speed digital, and high-power switch control peripherals, their

performance will be greatly affected by circuit board design. Please be sure to follow the PCB layout guidelines below to reduce unnecessary noise and improve the performance to the great extent.

The Σ-Δ filter module (SDF) is available on the G32R501 device, and is used in conjunction with an external Σ-Δ modulator for current measurement and rotary transformer position decoding in motor control applications. SDF uses an external clock through its SDF clock input pin. If the clock noise is particularly high, its operation will be disrupted easily. Special preventive actions should be taken for these signals to ensure the signals are clean and interference-free, and meet the SDF timing requirements detailed in the specific data sheet of the device. Therefore, it is recommended to use series termination resistors to cope with the ringing caused by any impedance mismatch of the clock driver, and to separate these leads from other high-noise signals. This helps to ensure proper functioning of SDF. Using the SDF synchronous GPIO (SYNC) option (synchronizing the clock pin with PLLRAWCLK) can provide protection and prevent SDF operations from being affected by occasional clock interference. It is important to note that the protection it receives is limited, so ensuring clock stability is the most importance for normal operation of SDF.

3.2.4 Communication peripherals

G32R501 device contains different quantities of the following universal peripherals:

(1) Controller area network (CAN)

(2) Internal integrated circuit (I2C)

(3) Power management bus (PMBus) interface

(4) Serial communication interface (UART)

(5) Serial peripheral interface (SPI)

(6) Local interconnection network (LIN)

(7) Quad serial peripheral interface (QSPI)

Considering the characteristics of these peripherals and their different communication modes, the communication peripherals that need to be supported must be fully considered in system design. The board-level interfaces (e.g. I2C, PMBus, and SPI) need to be connected to other components on the circuit board or to other devices through the circuit board. Due to the fact that these drivers usually run directly, special attention must be paid to their driving capability and wiring length during design. These factors are closely related to the frequency of the selected signal.

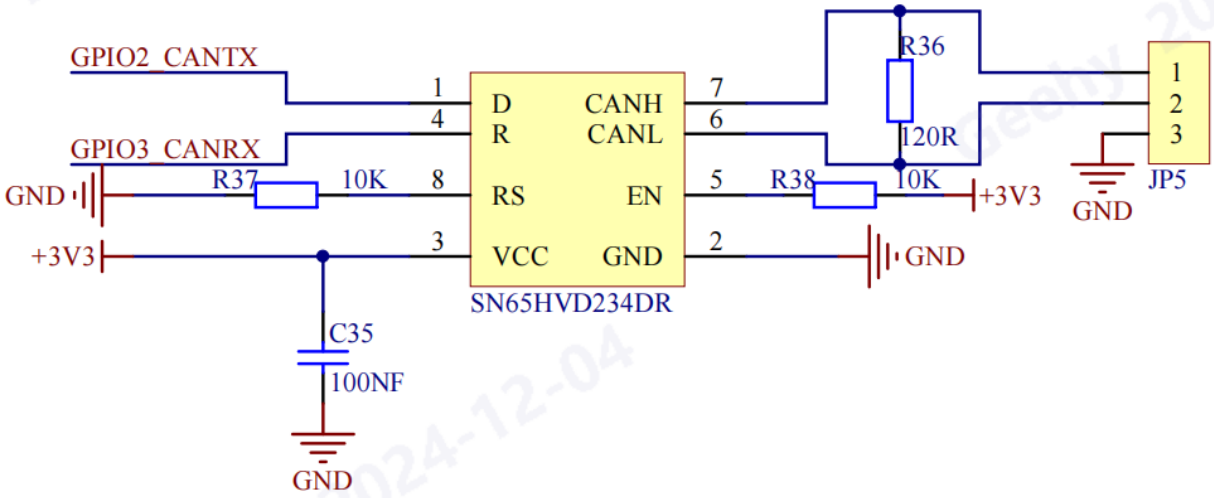
When CAN communication is used, it is recommended to use an external oscillator on the circuit board instead of relying on an internal oscillator. This is because the accuracy of on-chip zero-pin oscillators may not meet the requirements of CAN protocol for such parameters as bit

time setting, bit rate, bus length, and propagation delay.

For I2C interface, it is recommended to use external pull-up resistors on the SDAA and SCLA pins. If the pull-up resistor is too strong (i.e. the resistance is too low), the I2C pin will be hindered from being effectively driven to a low level; if the pull-up resistor is too weak (i.e. the resistance is too high), the communication speed will be affected. Therefore, when choosing the resistance value of the pull-up resistor, the balance between power consumption and speed shall be considered.

CAN and LIN interfaces can connect two or more circuit boards running on different processors. These ports usually require dedicated transceivers to convert electrical signals, in order to reduce noise, and ensure the communication with the ports on other devices. When using the communication transceivers, some transceivers may require adding a pull-up resistor to the communication pin of the MCU. This requirement can be verified according to the data sheet of the transceiver.

Figure 3 CAN Transceiver in G32R501 EVAL Diagram



UART is a flexible serial communication device, which supports full-duplex and half-duplex data exchange, compatible with the industry standard NRZ asynchronous serial data format. It provides a wide range of baud rate options and supports multiprocessor communication modes (in conjunction with protocols such as address frame).

The registers in this module are 16 bits wide, but only the lower 8 bits (bits 7-0) are valid. When accessing registers, the high bytes (bits 15-8) are always read as zero, and writing operations to high bytes are invalid.

3.2.5 Boot ROM and Peripheral Boot

The Boot ROM of G32R501 contains the Bootloader program, which will be executed every time the device is powered on or reset. GPO24 (Boot mode pin 1) and GPO32 (Boot mode pin 0) are Boot mode selection pins. Users can select Boot mode by changing the state of these pins. The

table below lists the Boot modes.

Table 1 Default Boot Mode for the Device

Boot mode	GPIO24 (Default boot mode selection pin 1)	GPIO32 (Default boot mode selection pin 0)
UART/Wait for boot	0	1
CAN	1	0
Flash	1	1

The default boot mode pins are GPO24 (boot mode pin 1) and GPO32 (boot mode pin 0). If users also use peripherals on these pins, the boot mode pin can be selected and set to weak pull-up, so the pull-up may be overdriven. On this device, customers can change the default boot mode pin by programming the user-configurable dual-code security module (DCS) OTP position.

3.3 Power System Design

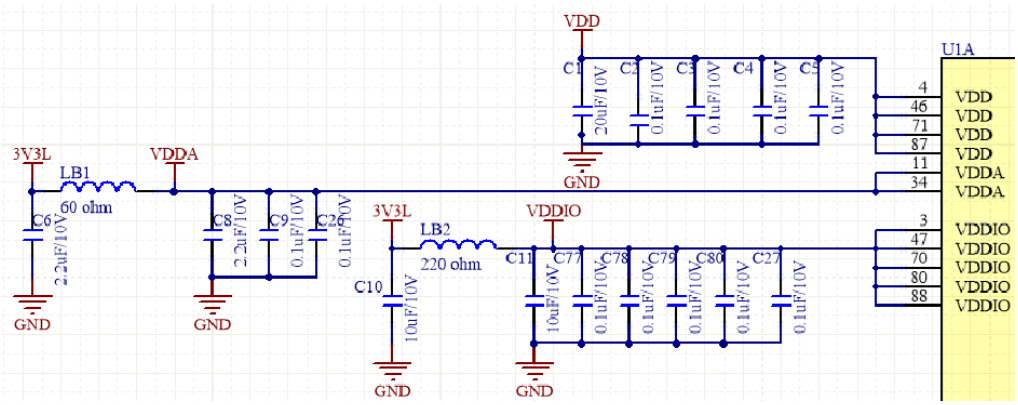
- G32R501 has multiple power pins, including:
- Core power pin (VDD)
- Analog power pin (VDDA)
- Digital I/O power pin (VDDIO)

To ensure the device functions properly, all available power pins must be correctly connected to the appropriate supply voltage. These power supplies include 3.3V and 1.1V. The core power pin (VDD) requires a voltage of 1.1V, which can be provided in various ways. 1.1V can be generated by on-chip LDO or provided externally, When the ambient temperature is within the typical industrial range (e.g., -40°C to 105°C), the built-in LDO can directly supply power to the VDD pin. To ensure stable operation of the chip in high-temperature environments ranging from 105°C to 125°C, an external LDO regulator should be used to provide independent power to the VDD pin. For details, please refer to Chapter 3.3.3. Analog (VDDA) and digital I/O (VDDIO) require an external supply of 3.3V.

3.3.1 Power supply requirements

An important aspect of ensuring power stability and noise resistance of the device is that each power pin has a grounded decoupling/bypass capacitor. These help to limit the propagation of noise to other areas of the system, especially the low-level analog signals. The decoupling capacitors serve as filters and temporary energy storage devices, effectively reducing the voltage drop/spike on the power supply and providing a more stable power solution for the device.

Figure 4 Decoupling Capacitors on Power Pins



3.3.2 Power-on sequence

Before the chip is powered on, the voltage on any digital pin should not exceed 4.125V, nor be lower than -0.3V; the voltage on any analog pin (including VREFHI) should not exceed 4.125V, nor be lower than -0.3V.

To be brief, it is necessary to drive the signal pin after XRSn changes to a high level, provided that all 3.3V power rails are connected together. Even if VDDIO and VDDA are not connected together, the timing control is still required.

Note: If the above timing is violated, current may flow through unexpected parasitic paths in the chip, causing failures or damage to the chip.

The acceptable power-on sequence for the power rails is summarized as follows. The “power on” here indicates that the relevant power rail has reached the recommended minimum operating voltage. The unacceptable sequences can lead to reliability problem and even damage to the device. To simplify the design, it is recommended to connect all 3.3V power rails together and operate according to the power-on sequence of power pins.

Table 2 External VREG Sequence Summary

Situation	Power-on sequence of power rails			Acceptable
	VDDIO	VDDA	VDD	
A	1	2	3	Yes
B	1	3	2	Yes
C	2	1	3	-
D	2	3	1	-
E	3	2	1	-
F	3	1	2	-
G	1	1	2	Yes

Situation	Power-on sequence of power rails			Acceptable
	VDDIO	VDDA	VDD	
H	2	2	1	-

Table 3 Internal VREG Sequence Summary

Situation	Power-on sequence of power rails		Acceptable
	VDDIO	VDDA	
A	1	2	Yes
B	2	1	-
C	1	1	Yes

Note: The analog module on the device should only be powered after VDDA reaches the recommended minimum operating voltage.

3.3.3 VDD voltage regulator

The internal VREG is powered by the VDDIO power rail, and connecting the VREGENZ pin to a low level can generate the 1.1V voltage required to power the VDD pin. The internal VREG can be used, and VDD does not need to be powered externally. However, to ensure VREG stability and avoid transient, decoupling capacitors are still needed on the VDD pin.

When using the internal VREG, the two recommended capacitor configurations for the VDD power rail are as follows:

- Place a small decoupling capacitor connected to VSS as close as possible to the device on each pin. In addition, a large-capacity capacitor connected to VSS must be placed on the VDD node. The recommended bypass capacitor configuration should be one 20μF capacitor or two parallel 10μF capacitors, as well as four 0.1μF capacitors connected in parallel.
- Evenly distribute the total capacitance connected to VSS on all VDD pins (divide the total capacitance by the number of available VDD pins).

When the internal voltage regulator is not used, the value of the decoupling capacitor is determined by the system voltage regulation solution.

To ensure stable operation of the chip at high temperature environments ranging from 105℃ to 125℃, the power supply system needs to be configured according to the following requirements.

Hardware configuration:

- Set the VREGENZ pin enable signal to a high level.
- Use an external LDO regulator to provide independent power supply for the VDD pin.

It is recommended to choose a linear voltage regulator that meets the following parameters:

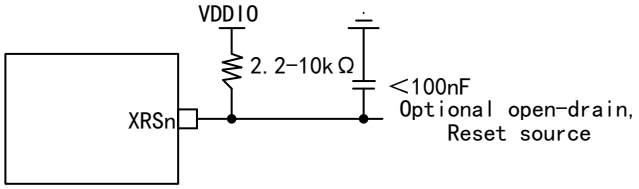
- Output voltage range: 1.1V-1.2V (adjustable or fixed output)
- Continuous output current: ≥ 300mA (meeting the peak load requirements)
- Operating temperature range: From -40℃ to +125℃ (covering the application environment temperature)
- Package form: It is recommended to use HTSSOP or QFN package with good heat dissipation performance

Note: In actual selection, thermal derating calculation shall be performed in combination with heat dissipation conditions of the system to ensure long-term reliability of LDO in high-temperature environment. For application scenarios of continuous high current, it is recommended to conduct thermal simulation verification.

3.4 XRSn and Reset System

XRSn is used as the reset pin for the chip. When powered on, the POR circuit built into the chip will pull down the XRSn pin, the watchdog (WWDT, NMIWDT) reset will also pull down the pin, and the external circuit may drive the pin to make the device reset take effect. It is recommended to place a resistor with a resistance of 2.2kΩ to 10kΩ between XRSn and VDDIO; and place a capacitor with a capacitance of less than 100nF between XRSn and VSS for noise filtering. When the watchdog reset takes effect, these values enable the watchdog to correctly drive the XRSn pin to VOL within 512 OSCCLK cycles. Figure 5 shows the recommended reset circuit.

Figure 5 Reset Circuit



3.5 Clock System Design

Correct clock generation is crucial for normal operation of the system, especially in real-time control systems. G32R501 provides flexible clock generation options, allowing users to adjust devices according to their specific system requirements. The chip is equipped with two 10MHz pin-free oscillators, supports on-chip crystal oscillators and external clock inputs, and has an on-chip phase-locked loop (PLL). Although the performance of the internal clock source is quite good, users can choose to use an external clock source to meet more accurate clock requirements. G32R501 supports three types of external clock methods: single-ended 3.3V external oscillator, external crystal, and external resonator.

3.5.1 Internal and External Oscillators

An important decision needs to be made in the design process, namely, whether to use the

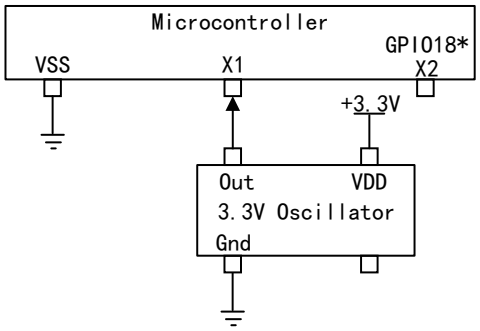
onboard clock option or integrate an external oscillator into the system. The following design precautions should provide adequate help in the decision-making process, but the final choice depends on cost and system clock requirements.

Two on-chip oscillators (INTOSC1 and INTOSC2) that do not require external pins operate at a frequency of 10MHz and can be used to provide clocks for the main PLL and CPU timer 2. In addition, INTOSC1 can also provide a clock for the watchdog module. When powered on, INTOSC2 is automatically set as the system reference clock source, while INTOSC1 serves as a backup clock, and they can seamlessly switch when the master clock fails, enhancing the system reliability. This clock option is very useful for the design that gives priority to cost saving and shortening of design cycle. Compared with external clock sources, the shortcoming of this decision is lower accuracy. The frequency stability of the internal oscillator is affected by the environment (temperature/voltage), with a typical deviation of ±1.5%~3% at 10MHz, which is lower than that of the external crystal (usually below ± 0.1%).

GPO18* and its multiplexer options can only be used when the system is timed by INTOSC and X1 has an external pull-down resistor. In addition to two on-chip oscillators that do not require external pins, it also supports three types of external clock sources:

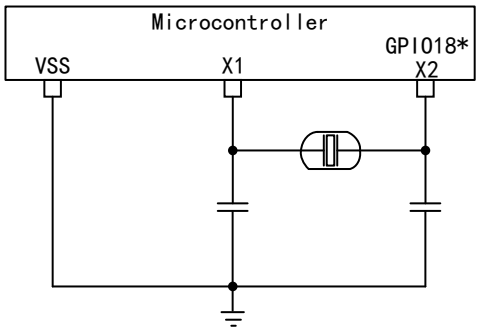
(1) Single-ended 3.3V external clock. The clock signal should be connected to X1 and XTALCR.SE bit should be set to 1.

Figure 6 Single-ended 3.3V External Clock



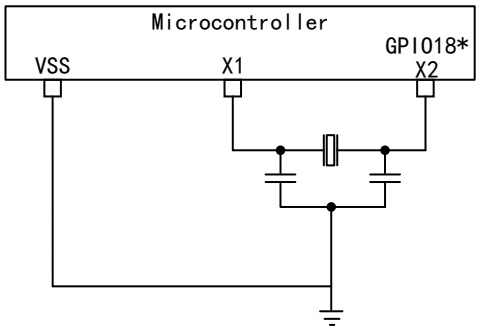
(2) External crystal. The crystal should be connected between X1 and X2, with its load capacitor connected to VSS.

Figure 7 External Crystal



(3) External resonator. The resonator should be connected between X1 and X2, and its ground terminal should be connected to VSS.

Figure 8 External Resonator



3.6 Debugging and Simulation

The G32R501 series provides rich debugging, tracking, and testing functions. They use standard Arm® CoreSight™ module configuration, and implement connection through daisy chain standard TAP controller. The debugging and tracking functions integrated into Arm® Cortex®-M52. The debugging system supports serial wire debugging (SWD) and tracking functions, in addition to standard JTAG debugging. For debugging and tracking functions, please refer to the following document: *Technical Reference Manual for Arm China Processor*.

The JTAG (IEEE 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. cJTAG (IEEE Standard 1149.7-2009 Reduced Pin and Enhanced Functionality Test Access Port and Boundary Scan Architecture) port is a compact JTAG interface that only requires two pins (TMS and TCK), which can serve other device function of multiplexing into traditional GPO35 (TDI) and GPO37 (TDO) pins.

Generally, it is recommended that the distance between the MCU target and the JTAG connector should not be less than 15cm, and there are no other devices on the JTAG chain, no buffer is required on the JTAG signal. Otherwise, every signal should be buffered. Besides, for most JTAG debugging probe operations at 10MHz, no series resistor is needed on the JTAG signal. However, if high simulation speed (around 35MHz) is required, a 22Ω resistor should be connected in series to each JTAG signal.

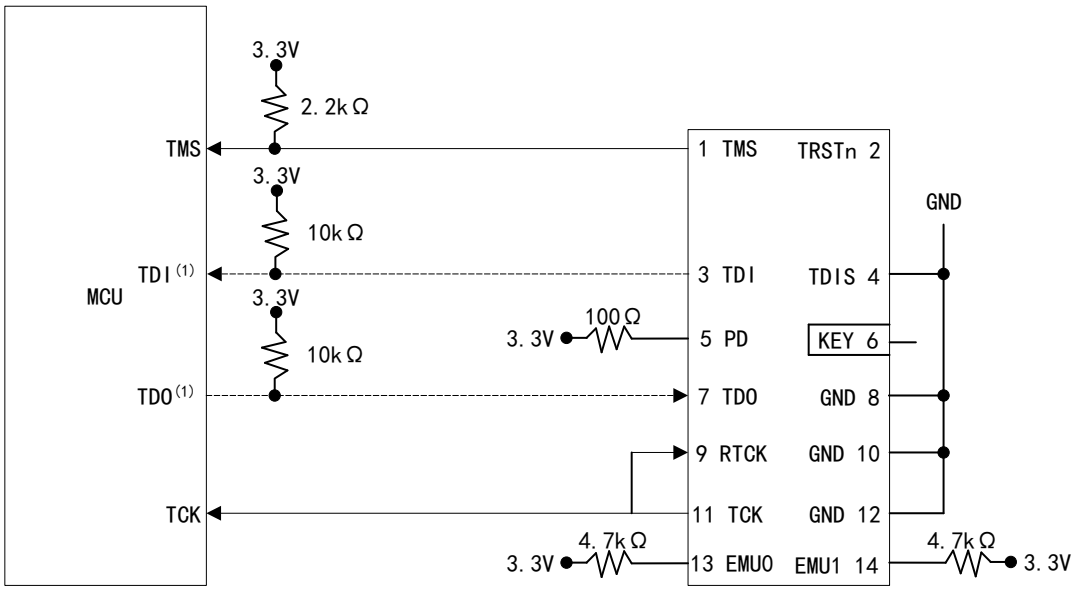
The PD (power detection) terminal of the JTAG debugging probe should be connected to 3.3V power supply of the circuit board. The GND terminal of the connector should be connected to the circuit board ground. TDIS (cable disconnect sensor) should also be connected to the circuit board ground. The JTAG clock should be looped back from the TCK output terminal of the connector to the RTCK input terminal of the connector (in order to detect the clock continuity through JTAG debugging probe). This MCU does not support EMU0 and EMU1 signals on 14-pin and 20-pin simulation connectors. These signals should always be pulled up at the simulation connector through a pair of on-board pull-up resistors ranging from 2.2kΩ to 4.7kΩ (depending on the driving strength of the debugger port). Usually a resistance of 2.2kΩ is used.

Terminal reset of the connector is open-drain output of the JTAG debugging probe connector, and through the JTAG debugging probe command, the circuit board components are reset (only available through the 20-pin connectors).

JTAG test data input (TDI) is the default multiplexer selection for pins. By default, the internal pull-up resistor is disabled. If this pin serves as JTAG TDI, an internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid suspension of input. In cJTAG option, this pin can serve as GPIO.

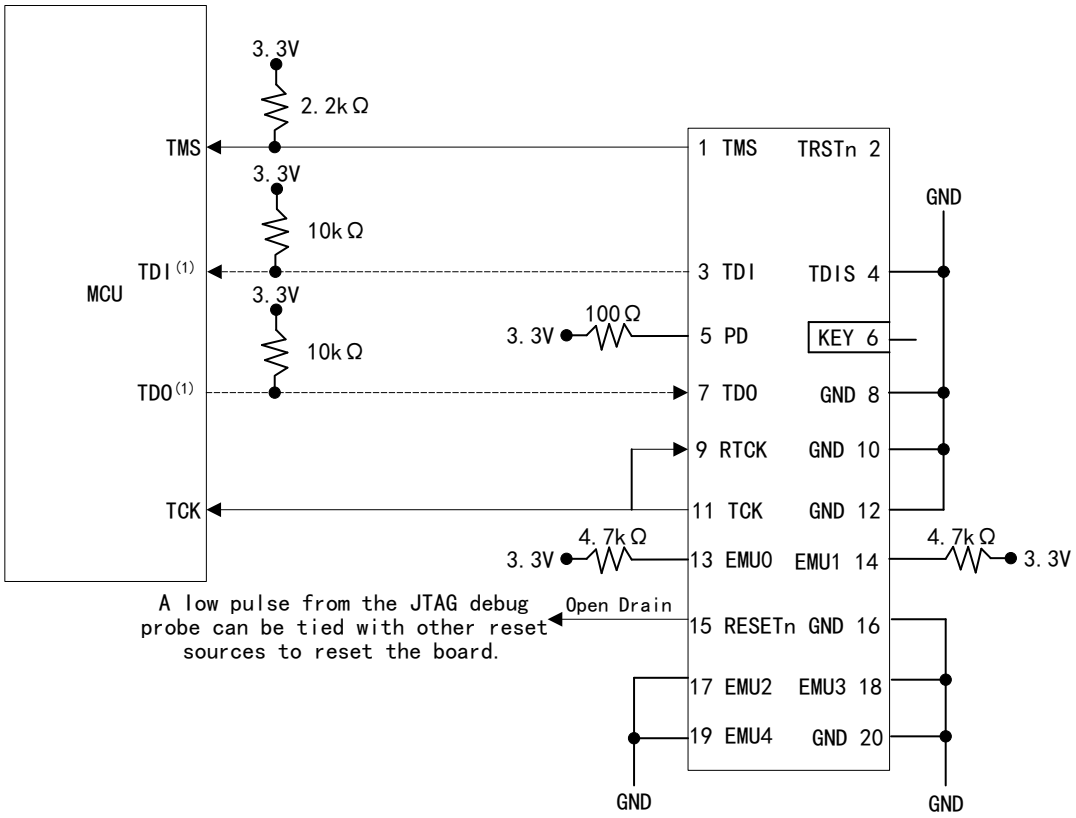
JTAG test data output (TDO) is the default multiplexer selection for pins. By default, the internal pull-up resistor is disabled. When there is no JTAG activity, the TDO function will be in a three-state condition, causing this pin to be suspended. An internal pull-up resistor should be enabled or an external pull-up resistor should be added on the circuit board to avoid suspension of input. In cJTAG option, this pin can serve as GPIO.

Figure 9 Connect to JTAG Connector of No. 14 Pin



Note: cJTAG option does not require connection of TDI and TDO, and these pins can be used as GPIO.

Figure 10 Connect to JTAG Connector of No. 20



Note: cJTAG option does not require connection of TDI and TDO, and these pins can be used as GPIO.

3.7 Handling of Unused Pins

For applications that do not need to use all functions of the device, the acceptable conditions for any unused pins are listed in the following table. When multiple options are listed, any option is acceptable.

Table 4 Connection of Unused Pins

Signal name	Acceptable practice
Analog	
Analog input pin with DACx_OUT	No connection Connect to VSSA through a resistor of 4.7kΩ or greater
Analog input pins (except for DACx_OUT)	No connection Bound to VSSA Connect to VSSA through a resistor
VREFHIx	Connect to VDDA (only applicable when ADC or DAC is not used in the application)
VREFLOx	Bound to VSSA
Digital	
GPIOx	No connection (enable the input mode of internal pull-up resistor)

Signal name	Acceptable practice
	No connection (disable the output mode of internal pull-up resistor) Pull-up or pull-down resistor (resistor of any value, input mode, disable internal pull-up resistor)
GPIO35/TDI	When selecting the TDI multiplexer option (default), GPIO is in input mode. Enable the internal pull-up resistor External pull-up resistor
GPIO37/TDO	When the TDO multiplexing option is selected (default), GPIO is in output mode only during JTAG activity; otherwise, it is in a three-state condition. This pin must be biased to avoid generating extra current on the input buffer. Enable the internal pull-up resistor External pull-up resistor
TCK	No connection Pull-up resistor
TMS	Pull-up resistor
VREGENZ	Connected to VSS
X1	Connected to VSS
GPIO18/X2	Turn off XTAL and: Enable the input mode of internal pull-up resistor External pull-up or pull-down resistor (input mode) Disable the output mode of internal pull-up resistor
Power supply and grounding	
VDD	All VDD pins must be connected as described in "Pin Signal Description".
VDDA	If no dedicated analog power supply is used, connect to VDDIO.
VDDIO	All VDDIO pins must be connected as described in "Pin Signal Description".
VSS	All VSS pins must be connected to the circuit board ground.
VSSIO	Always connect to VSS.
VSSA	If analog grounding is not used, connect to VSS.

4 PCB Layout Design Reference

After creating a system diagram and verifying its correct design and compliance with all engineering specifications, the next step is to create the PCB layout in your preferred PCB design software. The placement of components is crucial for achieving good design and device performance.

4.1 Introduction to Layout Design

In addition to wiring of all connections in the diagram design, good layout practices are also required to ensure the normal functions and reliability of the circuit board. All aspects of the circuit board (including physical dimensions, board limitations, and critical components) should be fully considered.

4.1.1 Recommended layout practice

The entire system of G32R501 usually includes the following circuits: low-level analog circuits, high-speed digital circuits, and high-power (switching) circuits. These three different types of signals should be separated from each other on the PCB. The high-current paths and high-frequency signals are particularly destructive to any analog signals on the circuit board.

4.1.2 Size of circuit boards

The size of the circuit board is highly dependent on the system being constructed and the application being implemented by G32R501. From small boards composed of a few components to large boards with a large number of components, PCB has a wide range. If possible, sufficiently large PCB can be allocated to make the layout design process as simple as possible and help with routing and separating different types of signals.

4.1.3 PCB stacking

Selection of the number of layers and layer stack of the circuit board depends on the required number of connections on the PCB and the production cost of the PCB. The circuit board with 4 or more layers is usually the best choice for G32R501 devices. This enables designers to achieve clean ground planes and segmented power planes. In terms of configuration, two diagrams are used to illustrate common 4-layer and 6-layer circuit board stacks. The 4-layer circuit board stack includes signal/component layer, ground plane, segmented power plane (3.3V, 1.1V, etc.), and signal/component layer. The stack of the 6-layer circuit board is as follows: signal/component layer, ground plane, segmented power plane (3.3V, 1.1V, etc.), signal layer, another ground plane, and signal/component layer.

Figure 11 Layer Stack of 4-Layer Circuit Board

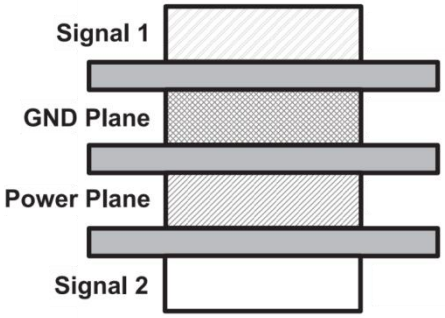
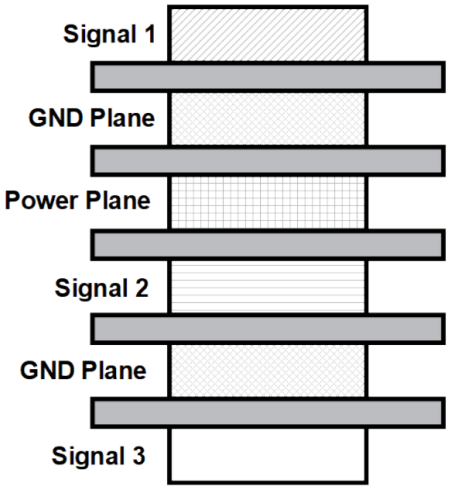


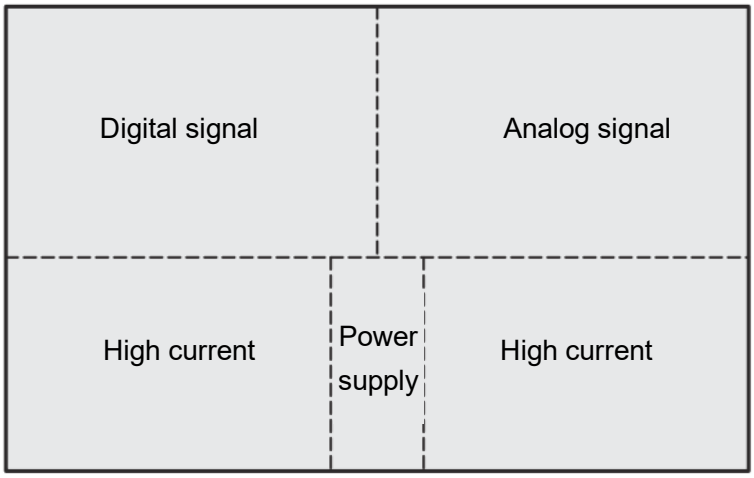
Figure 12 Layer Stack of 6-Layer Circuit Board



4.2 Recommended Circuit Board Layout and Wiring

A good practice to ensure that the signals arranged on the circuit board do not cause any crosstalk or performance degradation is to partition the circuit board, similar to that shown in Figure 13. As mentioned earlier, the four signals on the PCB (power supply, digital, analog, and high current) should be separated from each other.

Figure 13 Ideal Circuit Board Partitioning



4.3 Placement of Components

After the position of the G32R501 chip on the circuit board is determined, the next component to be placed is the crystal/oscillator. It should be placed as close as possible to the device to ensure the most effective clock solution is realized. Specifically, the leads to X1/X2 should be as short as possible. According to the additional components required for the specific crystal used, the crystal/resonator can be wired on the circuit board in different ways. When wiring the clock traces between devices, try using the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including low-frequency clocks, can have fast rise and fall time. The 3W rule can be adopted to reduce crosstalk between traces. Generally speaking, a certain space should also be maintained between parallel traces between devices. Avoid using right angles to arrange wiring, in order to greatly reduce the length of wiring and the discontinuity of impedance. To further protect the device from crosstalk, try to arrange protective traces (from GND pin to GND pin) on the side of the clock signal line as much as possible. This can reduce clock signal coupling.

The next most important component to be placed is the decoupling/bypass capacitor. These capacitors should be placed as close as possible to their respective pins to further reduce noise and help ensure power supply stability of the device. The decoupling capacitors that are more than one inch away from the pins have poor performance. On the other hand, the high-capacity capacitors can be placed far away from the chip without significantly affecting their performance.

The other components that should be followed next are JTAG/cJTAG connectors/circuits and XRSn circuits.

4.3.1 Precautions for power electronic components

The noise of power electronic components is very loud, which can seriously affect the performance of the device. These components and their signals are an important factor for the

placement of other types of signals. Any high-current path should be designed with a small loop area. Any high di/dt current should not pass through other di/dt paths, any sensitive analog signals, control circuits, or any test points. Any current detection operational amplifier can be placed in two ways. They can be placed next to the shunt, near the G32R501 chip for low-pass filtering, and connected to the analog ground (VSSA). Alternatively, they can be placed next to the G32R501 chip, and routed differentially to an operational amplifier using Kelvin detection.

Another note is that the radiator may have high dV/dt and should be grounded externally. Wiring the radiator to the circuit board ground may cause the radiator to be electrified. Any gate driver should be located near the FET.

4.4 Ground Layer

The copper surface on the PCB is an excellent high-frequency capacitor, and it can be used together with the recommended capacitors for high-frequency bypass. Another advantage of the solid plane is that they can serve as good radiators to reduce high heat level.

If the circuit board has enough layers, a good practice is to place a ground plane on the PCB. This ground plane not only helps to route the ground signals on the circuit board, but also helps to reduce the grounded noise. Each signal on the circuit board has a return current (via GND), which ensures that the return path passes through the path with the lowest impedance. For circuit boards with multiple ground planes on different layers, using via-hole splicing to connect these ground planes and further minimize the impedance is very useful.

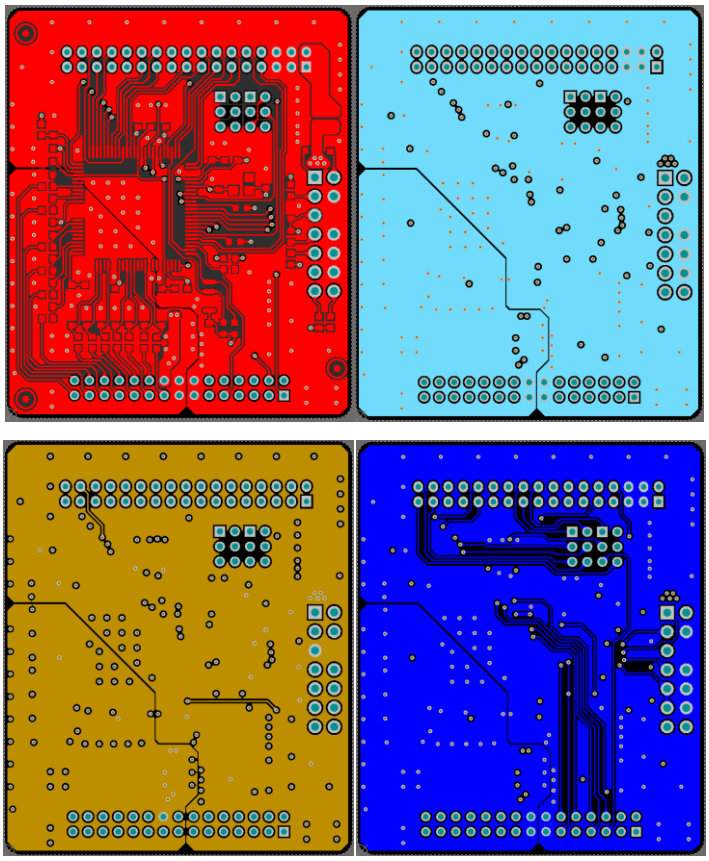
4.5 Design of Analog Signals and Digital Signals

It is repeated that, it is a good practice to separate analog ground from digital ground (and their power supplies). However, if it is not done well, it may lead to a decrease in the performance. The advantage of analog/digital separation is that it ensures that signals do not cross the isolation boundary unless the crossed signal is static. The separated signal should only be connected at one point, ideally the signal source. This kind of connection can be ferrite beads, simple resistors, or even breakpoints in a plane. Please note that ferrite beads provide negligible capacitance and low DC resistance. When choosing to use ferrite beads, appropriate simulations should be conducted to ensure that the ferrite beads can correctly filter out noise and do not restrict the current flowing to the device. If appropriate analog and digital separation cannot be achieved, designers should consider using only one ground plane.

The G32R501 device is designed to have an "analog angle", where all analog pins of the device are located. Many input sources in these ADC inputs usually come from the power electronics components in the design. This area is usually the noisiest part of the circuit board, and it can seriously affect the simulation performance. It is best to minimize the analog ground area and make the analog ground close to the G32R501 chip to prevent noise from affecting the ADC of the device. Correctly reducing the size of the analog ground plane can reduce the noise pickup.

Below is an example of analog/digital separation.

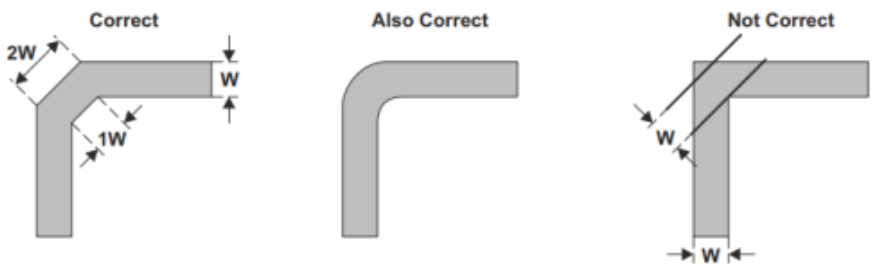
Figure 14 Segmentation Diagram of Analog Signals and Digital Signals on 4-layer PCB



4.6 Lead and Via-hole Design for Signal Wiring

To implement proper signal wiring, please ensure that all leads are not bent at a 90° angle. Although this is automatically set in most PCB design software, confirming this property in all leads is a good practice. The lead should be arranged at a maximum angle of 45° or along a curve as much as possible to reduce the reflection and characteristic impedance changes along the lead, and thereby reduce the radiation. This is because a right angle will cause an increase in capacitance in the corner area, resulting in impedance changes and reflection. Besides, a good practice is to make the signals on adjacent layers perpendicular to each other (at a 90° angle). This can reduce crosstalk between signals and ensure minimal interference between signals. Leaving sufficient spacing between leads can also reduce crosstalk, especially for the signals with a short rise/fall time.

Figure 15 Appropriate Signal Wiring Leads



4.7 Precautions for Heat Dissipation

For each G32R501, there are detailed records for its thermal characteristics and temperature specification limitations. Any system and final product that exceeds the maximum power dissipation recommended in the data sheet may require additional heat dissipation in the design. The main consideration for heat dissipation is junction temperature (TJ). This specification should be carefully tested to maintain it within the absolute and recommended limits. This can ensure that the device remains reliable and functions normally throughout its entire lifespan. Another consideration for heat dissipation is ambient temperature (TA), but this depends on the final application environment and product design.

In order to minimize TJ through PCB design, the system design should ensure that the thermal resistance from the board to the environment is very small. GND and power pins are the main methods for heat dissipation of the device. Therefore, if the device has heat dissipation pad pins, please ensure that they are connected to the large copper clad area on the PCB. In most packages, the heat dissipation pad will be connected to the GND inside the device or externally connected to GND. Similarly, please ensure that any GND and power pads are connected well to the solid plane, and that any via-hole is close to the G32R501 device.

5 Precautions for ESD and EOS, EMI/EMC

5.1 Electrostatic Discharge

The accumulation of charges may lead to electrostatic discharge (ESD) during the operation of the device. Special care is required when handling and storing these MCU. All G32R501 devices have been tested: HBM complies with ANSI/ESDA/JEDEC JS-001 standard (1), and CDM complies with JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2).

Table 5 ESD Absolute Maximum Ratings

Symbol		Parameter	Condition	Pin	Range	Unit
100 pins						
V (ESD)	Electrostatic Discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
80 pins						
V (ESD)	Electrostatic Discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
64 pins						
V (ESD)	Electrostatic Discharge	Human body model (HBM); conform to ANSI/ESDA/JEDEC JS-001 standard (1)			±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)	All pins	±1000	
56 pins						
V (ESD)	Electrostatic Discharge	Human body model (HBM)	Conform to ANSI/ESDA/JEDEC JS-001 standard (1)		±4000	V
		Charging device model (CDM)	Conform to JEDEC, JESD22-C101 or ANSI/ESDA/JEDEC JS-002 (2)		±1000	

The supply voltage interference or electrostatic discharge (ESD) may cause the device to enter an unknown state. Therefore, adopting a good PCB layout is crucial in order to ensure excellent noise and ESD performance. In addition, similar ESD protection diodes can be used on the cJTAG pin. The loop area of key pins (e.g. cJTAG, XRS, X1, X2) shall be minimized as much as possible. If any pins (e.g. GPIO) need to be connected to an external connector in the design, be sure to handle ESD issues carefully by adding ESD protection components. In some cases, mechanical methods (e.g. metal shielding or rewiring, etc.) may be required to enhance ESD protection. When using these external ESD protection devices, please strictly follow the layout guidelines provided in the specific device data sheet to ensure their effectiveness.

5.2 Electromagnetic Compatibility and Electromagnetic Interference

Electromagnetic compatibility (EMC) describes the ability of electronic components to function properly under the interference from other systems. Between them, the most important consideration is electromagnetic interference (EMI), namely the radio frequency energy emitted by the devices and other devices nearby. This interference can propagate and affect the device through conduction and radiation.

Therefore, when designing the system, ensure that the EMI emitted by the circuit board through radiation and conduction does not exceed the maximum value allowed by the specified standards. The hardware designers shall strive to reduce the radiated and conducted EMI to a level far below the certification limit. Similarly, the design of the circuit board shall have sufficient shielding so that it can function properly even when exposed to radiation and conducted electromagnetic energy from other surrounding systems.

Most components in the system, including PCB, connectors, cables, etc., are sources of EMI. Especially when designing the circuit boards that use high-frequency and fast switching currents and voltages, all wiring essentially serves as antennas that radiate electromagnetic energy. The five main radiation sources are: digital signals propagating on the wiring, current return loop area, insufficient power filtering or decoupling, impact of transmission lines, and missing power plane and ground plane. The fast switching clock, external bus, and PWM signal are used as control output in switching power supply. Power supply is another main source of EMI. RF signals can propagate from one part of the circuit board to another, thereby increasing the EMI. The energy radiated by switching power supply may result in failure to pass EMI test.

To reduce any harmful EMI generated by the circuit board and its components, please comply with the following guidelines throughout the diagram and layout design process:

- Use multiple decoupling capacitors with different capacitance values and appropriate power decoupling techniques. Please note that each capacitor has a self-resonant frequency.
- Use appropriate filtering capacitors on the power supply. These capacitors and decoupling capacitors should have low equivalent series inductance (ESL).
- If there is available space on the wiring layer, create a ground plane. Connect these ground areas to the ground plane using via-holes; creating via-hole grids with one quarter of inch is an ideal choice.
- High-frequency signals (low address lines, clock signals, serial ports, etc.) are usually connected to CMOS input end, and this input are parallel load greater than 100K, usually 10pF. Charging/discharging of such loads can result in high current peaks. One possible solution is to add a series termination resistor (approximately 50Ω) and finely tune it to realize ideal signal integrity. According to the transmission line theory, if the total output resistance (internal + external) is less than the line impedance (usually 70Ω -120Ω), it will have no negative impact on the speed. Usually, if timing is not critical, the rise time of the signal can be shortened by adding a series termination resistor. This method can bring

significant benefits at a low cost.

- Usually, the PWM signal driving the three-phase H-bridge switch can cause current spikes. Compared with asymmetric PWM, the symmetric PWM can reduce EMI related to dU/dt and di/dt by about 66%. Space vector PWM is also symmetrical relative to PWM period. However, since there are only two transistors for switching during one PWM period, the switching loss and EMI radiation are reduced by 30% compared to symmetric PWM.
- Minimize the current loop. Add as many decoupling capacitors as possible. Always apply the current return rule to reduce the loop area.
- Keep the high-speed signals away from other signals, especially from input and output ports or connectors.
- Apply the current return rule to connect the ground together while isolating the ground plane of the analog part. If the project does not use ADC and there is no analog circuit, do not isolate the ground.
- Avoid using ferrite beads to connect the divided ground. At a high frequency, ferrite beads have high impedance and generate significant ground potential difference between the plane or PC board stack, so as many power planes and ground planes as possible should be added. Place the power plane and ground plane adjacent to each other to ensure a stack with low impedance or high inherent capacitance.
- Use a π-type filter that suppresses EMI for all signals entering and exiting the system.
- If the system fails to pass the EMI test, trace the frequency source that did not pass to find the cause. For example, assume that the design fails at 300MHz, but there are no components on the circuit board operating at this frequency. The reason may be that the 100MHz signal generated a third harmonic.
- Determine whether the failed frequency is common mode or differential mode. Remove all cables connected to the system. If there is a change in the radiation, it is common mode. If there is no change, it is a differential mode. After identifying the cause, use termination or decoupling techniques to reduce the radiation. If it is common mode, add a π-type filter to the input and output. Adding a common mode choke to the cable is an effective solution, but this method of reducing EMI has a high cost.

6 Revision

Table 6 Document Revision History

Date	Version	Change History
April, 2025	1.0	New
September,2025	1.1	Modify the description and schematic of the decoupling capacitor on the power pins.

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